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Question Paper Code : 40192

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Sixth Semester

Electronics and Communication Engineering

EC 1354 — VLSI DESIGN

(Common to Electrical and Electronics Engineering)

(Regulations 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the special feature of Twin-Tub process?
2. Differentiate Enhancement and Depletion mode device.
3. Draw stick encoding diagram for two input NOR gate.
4. Design 2:1 MUX using transmission gate.
5. Draw the transfer characteristics of a CMOS inverter.
6. How do you overcome short channel effects in MOS transistors?
7. Draw the circuit diagram and truth table of Modulo 2 Adder.
8. Define the term crosstalk.
9. Distinguish between behavioural modeling and data flow modeling.
10. What is test bench?

PART B — (5 × 16 = 80 marks)

11. (a) Explain the various steps involved in Twin-tub fabrication process for an inverter.

Or

(b). Draw and discuss the MOS transistor Model and small signal AC characteristics with neat diagrams.

12. (a) Explain the complimentary CMOS inverter DC characteristics. (16)

Or

(b) (i) Explain the concept of static and dynamic CMOS design. (8)

(ii) Explain the construction and operation of transmission gates. (8)

13. (a) (i) Explain in detail about the scaling concept and design margin concepts. (12)

(ii) Write short notes about the transistor sizing for the performance in combinational Networks. (4)

Or

(b) Describe in detail about the resistance and capacitance estimation combination in a CMOS circuit with the proper loads and drivers. (16)

14. (a) (i) Design a generic carry look ahead adder. (10)

(ii) Explain briefly about high speed adder circuits. (6)

Or

(b) (i) Design a circuit for a 4 bit unsigned magnitude comparator and explain. (8)

(ii) Describe about delay modeling and clock distribution in ICs. (8)

15. (a) Explain in detail about hierarchical modeling concepts with suitable examples in VHDL. (16)

Or

(b) (i) Explain the Task and-functions in VHDL with an examples. (8)

(ii) Briefly explain dataflow and behavioural level modeling in VHDL. (8)
